CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system comprising:

a media access controller (MAC); and

a communication device comprising:

a media independent interface (MII) coupled to the MAC to at least one of transmit and receive data at a data rate;

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

a transmitter coupled to the MII to receive data from the MII and coupled to selectively transmit the data to one or more of the data lane interfaces at a variable rate dependent upon a number of the data lane interfaces to which the transmitter is transmitting the data<u>, wherein the transmitter is coupled to receive a transmit clock signal having a variable frequency dependent upon the number of the data lane interfaces actively transmitting a serial data signal</u>.

2. (Original) The system of claim 1, wherein the system further comprises a switch fabric coupled to the MAC.

3. (Original) The system of claim 1, wherein the system further comprises a packet classification device coupled to the MAC.

4. (Currently Amendd) A device comprising:

a media independent interface (MII) to at least one of transmit and receive data at a data rate;

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

a receiver coupled to receive one or more of the serial data signals from one or more corresponding data lane interfaces, the receiver further coupled to transmit the data to the MII at a variable rate dependent upon a number of the data lane interfaces from which the receiver is receiving the one or more serial data signals, wherein the receiver is coupled to receive a receive clock signal having a variable frequency dependent upon the number of the data lane interfaces actively receiving a serial data signal.

5. (Original) The device of claim 4, wherein each data lane interface is associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal.

6. (Previously Presented) The device of claim 5, wherein the plurality of data lane interfaces are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface.

7. (Original) The device of claim 4, wherein the device further comprises:

a plurality of 8B10B decoders, each 8B10B decoder being associated with one of the data lane interfaces, each 8B10B decoder being capable of decoding one eight bit byte from a differential pair on first intervals of a first clock signal;

a receive state machine to provide a fixed length data signal to the MII on second intervals of a second clock signal; and

logic to vary the second intervals based upon a number of the data lane interfaces actively receiving serial data from the device-to-device interconnection.

8. (Original) The device of claim 4, wherein the device further comprises:

a transmit state machine to receive a fixed length data signal from the MII on first intervals of a first clock signal;

a plurality of 8B10B encoders, each 8B10B encoder being associated with one of the data lane interfaces, each 8B10B encoder being capable of encoding one eight bit byte of the fixed length data signal for transmission to a differential pair on first intervals of a first clock signal; and

logic to vary the second intervals based upon a number of the data lane interfaces actively transmitting serial data from to the device-to-device interconnection.

9. (Original) The device of claim 4, wherein the device-to-device interconnection comprises printed circuit board traces.

10. (Original) The device of claim 4, wherein the device-to-device interconnection comprises a cable.

11. (Currently Amended) A method comprising:

at least one of transmitting data to and receiving data from a media independent interface (MII) at a data rate;

at least one transmitting a serial data signal to and receiving a serial data signal from one or more data lanes in a device-to-device interconnection, each data lane being coupled to the MII by an associated data lane interface; [[and]]

varying the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection[[.]]<u>; and</u>

<u>generating a variable clock signal for timing the transmitting having a frequency based upon the number of data lane interfaces actively transmitting a serial data signal.</u>

12. (Original) The method of claim 11, the method further comprising:

transmitting one or more serial data signals to the device-to-device interconnection in a first differential pair signal; and

receiving one more serial data signals from the device-to-device interconnection in a second differential pair signal.

13. (Original) The method of claim 12, the method further comprising transmitting data to and receiving data from a 10 gigabit attachment unit interface.

14. (Original) The method of claim 11, wherein the method further comprises:

at one or more data lane interfaces, receiving a serial data signal from the device to device interconnection;

decoding the serial data signal according to an 8B10B decoding scheme to provide an eight-bit byte on byte intervals;

providing a fixed length data signal to the MII on intervals of a clock signal having a frequency; and

varying the frequency of the clock signal based upon a number of the data lane interfaces actively receiving a serial data signal from the device-to-device interconnection.

15. (Original) The method of claim 11, wherein the method further comprises:

receiving a fixed length data signal from the MII on intervals of a clock signal having a frequency, the fixed length data signal having a plurality of eight-bit bytes;

encoding each eight-bit byte into a ten bit code group according to an 8B10B encoding scheme;

transmitting the code groups to the device-to-device interconnection through one or more data lane interfaces; and

varying the frequency of the clock signal based, at least in part, upon a number of data lane interfaces actively transmitting serial data to the device-to-device interconnection.

16. (Original) The method of claim 11, wherein the device-to-device interconnection comprises printed circuit board traces.

17. (Original) The method of claim 11, wherein the device-to-device interconnection comprises a cable.

18. (Currently Amended) A system comprising:

a physical layer communication device to transmit data between a transmission medium and a media independent interface (MII) at a data rate; and

a communication device comprising:

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

a transmitter coupled to the MII to receive data from the MII and coupled to selectively transmit the data to one or more of the data lane interfaces at a variable rate dependent upon a number of the data lane interfaces to which the transmitter is transmitting the data, wherein the transmitter is coupled to receive a transmit clock signal having a variable frequency dependent upon the number of the data lane interfaces actively transmitting a serial data signal.

19. (Original) The system of claim 18, wherein the physical layer communication device is adapted to transmit data between the MII and a fiber optic cable.

20. (Previously Presented) The system of claim 18, wherein the physical layer communication device is adapted to transmit data between the MII and a twisted wire pair cable.

21. (Currently Amended) A device comprising:

a physical coding sublayer (PCS) including a state machine to at least one of transmit and receive data at a data rate;

a physical media dependent (PMD) section including a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection, wherein the PMD section is coupled to the PCS section to signal to the PCS section a number of the data lane interfaces actively transmitting a serial data signal; and

logic to vary the data rate based, at least in part, upon the number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection, wherein the state machine is coupled to receive a clock signal to time transmitting or receiving the data having a variable

frequency dependent upon a number of the plurality of data lane interfaces that are actively transmitting or receiving a serial data signal.

22. (Original) The device of claim 21, wherein each data lane interface is associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal.

23. (Original) The device of claim 22, wherein the plurality of data lane interface are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface.

24. (Cancelled)

25. (Cancelled)

26. (Original) The device of claim 21, wherein the device further comprises a MAC to at least one of transmit data to and receive data from the state machine at the data rate.

27. (Original) The device of claim 21, wherein the device further comprises a physical layer communication device to at least one of transmit data to and receive data from the state machine at the data rate.

28. (Original) The device of claim 21, wherein the device-to-device interconnection comprises printed circuit board traces.

29. (Previously Presented) The device of claim 21, wherein the device-to-device interconnection comprises a cable.

30. (Currently Amended) A method comprising:

at least one of transmitting data to and receiving data from a state machine at a data rate;

at least one transmitting a serial data signal to and receiving a serial data signal from one or more data lanes in a device-to-device interconnection, each data lane being coupled to the state machine by an associated data lane interface; [[and]]

varying the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or receiving a serial data signal from the device-to-device interconnection[[.]]; and

generating a variable clock signal for timing the receiving having a frequency based upon the number of data lane interfaces actively receiving a serial data signal.

31. (Original) The method of claim 30, the method further comprising:

transmitting one or more serial data signals to the device-to-device interconnection in a first differential pair signal; and

receiving one more serial data signals from the device-to-device interconnection in a second differential pair signal.

32. (Original) The method of claim 31, the method further comprising transmitting data to and receiving data from a 10 gigabit attachment unit interface.

33. (Currently Amended) The method of claim 30, wherein the device further comprises:

controlling the data rate according to a frequency of [[a]] the variable clock signal;

at one or more data lane interfaces, receiving a serial data signal from the device to device interconnection;

decoding the serial data signal according to an 8B10B decoding scheme to provide an eight-bit byte on byte intervals; and

varying the frequency of the variable clock signal based upon a number of the data lane interfaces actively receiving a serial data signal from the device-to-device interconnection.

34. (Currently Amended) The method of claim 30, wherein the method further comprises:

receiving a fixed length data signal at the state machine at a rate controlled by a transmit clock signal having a frequency, the fixed length data signal having a plurality of eight-bit bytes;

encoding each eight-bit byte into a ten bit code group according to an 8B10B encoding scheme;

transmitting the code groups to the device-to-device interconnection through one or more data lane interfaces; and

varying the frequency of the transmit clock signal based, at least in part, upon a number of data lane interface actively transmitting serial data to the device-to-device interconnection.

35. (Previously Presented) The system of claim 1, wherein the communication device further comprises:

a physical coding sublayer ("PCS") including the transmitter; and

a physical media dependent ("PMD") section including the plurality of data lane interfaces, the PMD section coupled to the PCS section to signal to the PCS section the number of the data lane interfaces actively transmitting a serial data signal.

36. (Currently Amended) The system of claim 35, wherein the transmitter comprises a state machine ~~and wherein the transmitter is coupled to receive a transmit clock signal (TX_CLK) having a frequency dependent upon the number of the data lane interfaces actively transmitting a serial data signal~~.